Migration from T89C51RD2 to AT89C51RD2/ED2

This application note is a guide to assist current T89C51RD2 users in converting existing designs to the AT89C51RD2/ED2 devices. In addition to the functional changes, the electrical characteristics of the AT89C51RD2/ED2 are different including an increase in operating power supply range. Check the datasheet for detailed information.

To permit an easy migration, this application note compares the features, memory organization/accesses, SFRs and bootloader functionality.

Feature Comparison

Description	T89C51RD2	AT89C51RD2/ED2
Program Memory	64K bytes (63K bytes user Flash memory and 1K bytes Flash bootloader)	Full 64K bytes program/code memory
In-System Programming (ISP)	1K byte Flash bootloader mapped in the upper 64K bytes user Flash including serial ISP and Flash API	2K bytes ROM bootloader overlapped with user Flash including fast serial ISP and Flash API
RAM	256 bytes	256 bytes
XRAM	1024 bytes	1792 bytes
On-Chip EEPROM data	2048 bytes 64 bytes page write	2048 bytes byte write (ED2 only)
16-bit Timers	Yes (3)	Yes (3)
X2 Mode	CPU & Programmable separately by peripherals	CPU & Programmable separately by peripherals
SPI Interface	No	Yes
Keyboard Interface	No	Yes (8 inputs)
Prescaler	No	Yes
Baud Rate Generator	No	Yes
Internal Interrupt sources	5	10
Maximum Frequency @ 5V	40 MHz X1 mode 20 MHz X2 mode	40 MHz X1 mode 20 MHz X2 mode
Power Supply	4.5 to 5.5V (M version) 2.7 to 3.3V (L version)	Unique Operating Voltage: 2.7V to 5.5V
Pinout	T89C51RD2 and AT89C51RD2/ED2 are pinout compatible.	

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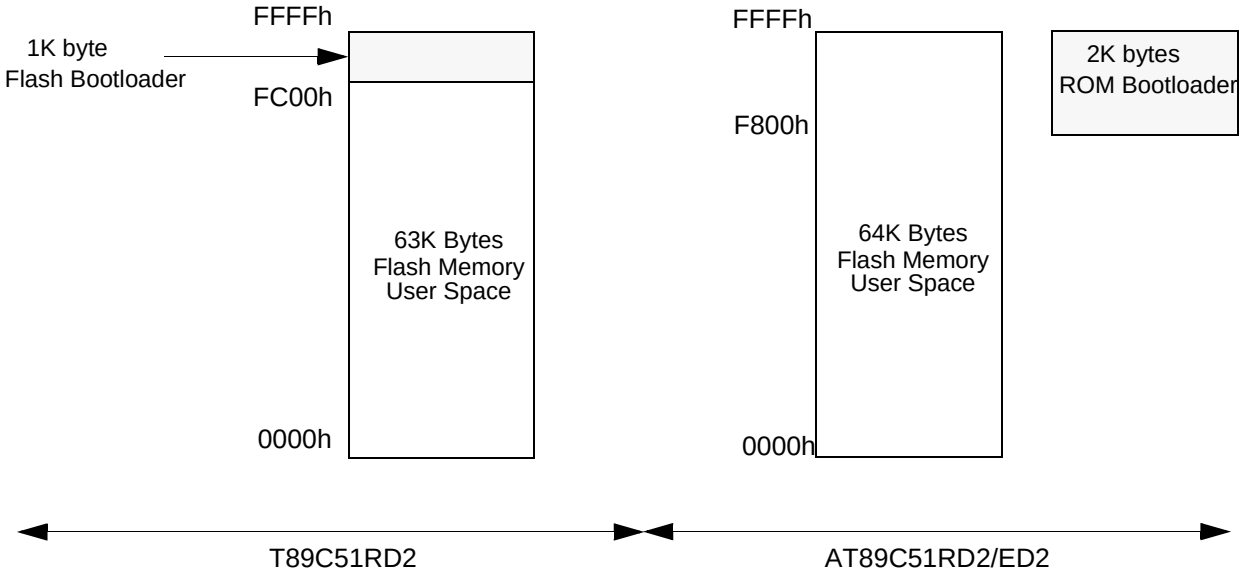
Memory Organization

Code Memory Organization

T89C51RD2 has a single 64K bytes code memory area including 63K bytes of program/code Flash memory and the upper 1K bytes dedicated for bootloader (serial ISP and Flash API).

The AT89C51RD2/ED2 implements 64K bytes of on-chip program/code memory and a standalone 2K bytes ROM for bootloader (serial ISP and Flash API). By default the microcontroller addresses the 64K bytes of on-chip Flash program/code memory. To address the upper 2K bytes ROM bootloader, the ENBOOT bit in AUXR1 register must be set (to access Flash API from user application for example).

Figure 1. Code Memory Organization



On-chip RAM/XRAM Memory

Both T89C51RD2 and AT89C51RD2/ED2 have 256 bytes of scratch pad RAM. The AT89C51RD2/ED2 has 1792 bytes of internal XRAM, whereas the T89C51RD2 has only 1024 bytes.

By default AT89C51RD2/ED2 has 768 bytes of on-chip XRAM selected after reset to ensure software compatibility with T89C51RD2.

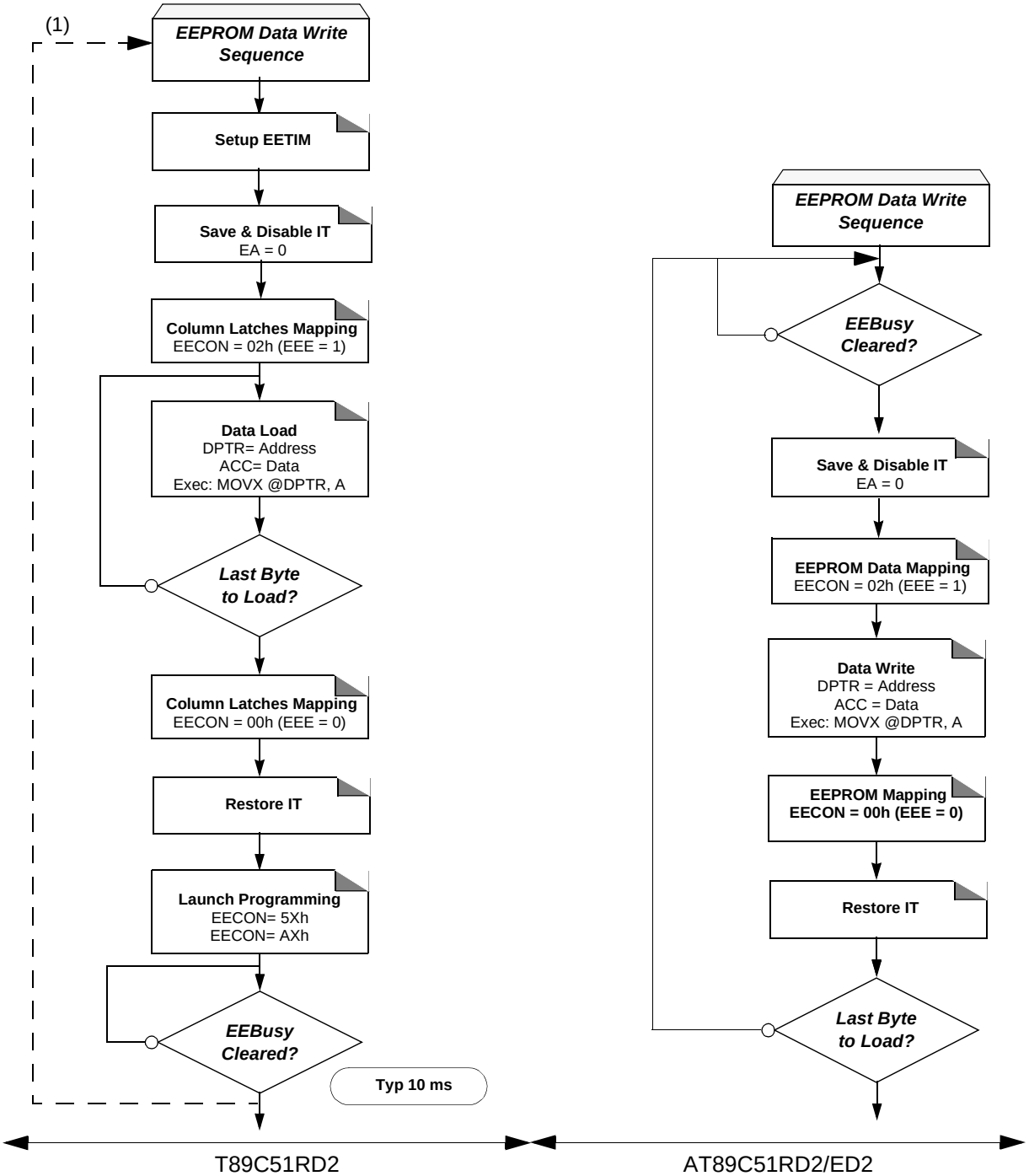
On-chip EEPROM Data

Both T89C51RD2 and AT89C51ED2 have 2K bytes of EEPROM for data storage. AT89C51RD2 has no on-chip EEPROM. Thus when migrating from an application using EEPROM data, the AT89C51ED2 device should be used.

EEPROM Data Write Access

The main difference between the products is the write activation sequence for the on-chip EEPROM data. AT89C51RD2/ED2 is single-write byte only access, thus no page write mode is available.

Figure 2. Recommended EEPROM Data Write Sequences



Note 1. Due to trouble T15 (see T89C51RD2 erratasheet), the write sequence may be executed 3 times.

As shown in Figure 2, EEPROM data in AT89C51ED2 is single byte access for read and write accesses.

Writing EEPROM data for AT89C51ED2 is simpler than in T89C51RD2:

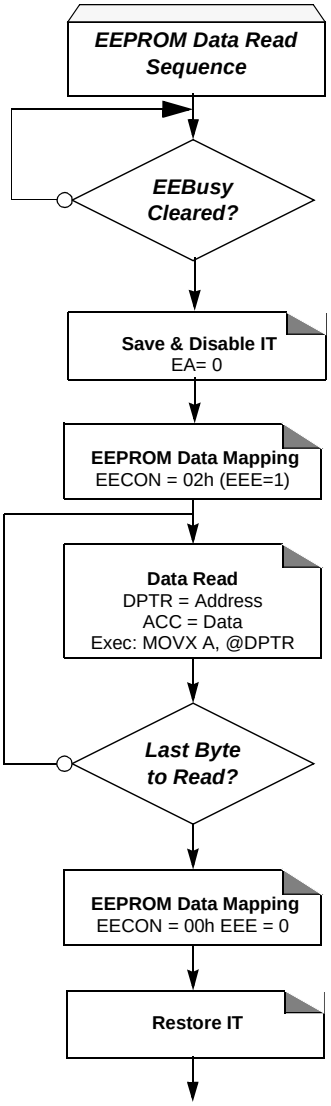
- Load DPTR with the EEPROM address
- Load ACC with the EEPROM data
- Set EEE bit
- Execute MOVX @DPTR, A
- Wait for EEBUSY flag to be clear before launching a new writing sequence

AT89C51ED2 does not need to setup any write time register as EETIM register for T89C51RD2. Write mechanism on EEPROM data is auto-timed and independent from the microcontroller running frequency.

EEPROM Data Read Access

The EEPROM data read sequence is the same between T89C51RD2 and AT89C51RD2/ED2 and does not imply any user software application modification.

Figure 3. Recommended EEPROM Data Read Sequence for Both Products



Hardware Configuration Byte (HSB)

The Hardware Configuration Byte defines the start-up conditions at reset:

- enable or disable X2 mode (X2 bit)
- enable or disable on-chip XRAM
- force bootloader execution after reset (BLJB: Bootloader Jump Bit)

For T89C51RD2 HSB is accessible using parallel programmers. The AT89C51RD2/ED2 introduces the capability to change X2 and BLJB bits from ISP or In Application Programming (self-programming), all other bits (XRAM, and LB3:1) remain accessible using parallel programming only (like T89C51RD2).

Table 1. Hardware Configuration Byte (HSB)

HSB	7	6	5	4	3	2	1	0
T89C51RD2		BLJB	BLLB	-		LB3	LB2	LB1
AT89C51RD2/ED2	X2	BLJB	-	-	XRAM	LB3	LB2	LB1

AT89C51RD2/ED2 features a new XRAM bit to disable the on-chip XRAM. There is no BLLB bit in the AT89C51RD2/ED2 since bootloader code is in ROM memory and there is no need to protect it from hazardous write sequences. As HSB byte has no software access on T89C51RD2, the AT89C51RD2/ED2 HSB behavior does not require application modification.

SFR Mapping

Table 2 contains an SFR comparison between previous and new products.

Table 2. SFR Mapping

	Bit Addressable	**Non Bit Addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAP2H XXXX XXXX	CCAP3H XXXX XXXX	CCAP4H XXXX XXXX		FFh
F0h	B 0000 0000								F7h
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAP2L XXXX XXXX	CCAP3L XXXX XXXX	CCAP4L XXXX XXXX		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000	FCON XXXX 0000	EECON xxxx xx00						D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h	P4 1111 1111			SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX		P5 byte Addressable 1111 1111	C7h
B8h	IPL0 X000 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111	IEN1 XXXX X000	IPL1 XXXX X000	IPH1 XXXX X111				IPH0 X000 0000	B7h
A8h	IEN0 0000 0000	SADDR 0000 0000						CKCON1 XXXX XXX0	AFh
A0h	P2 1111 1111		AUXR1 XXXX X0X0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	KBLS 0000 0000	KBE 0000 0000	KBF 0000 0000		9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XX00 1000	CKCON0 0000 0000	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Modified Registers

New Registers

Modified Registers

For modified SFR, the reset value may have changed from T89C51RD2. The AT89C51RD2/ED2 introduces several new bits in these SFR in place of reserved bits. Thus, if the software application on T89C51RD2 ignores these bits (logically masked), no code modification is needed to use AT89C51RD2/ED2 devices.

Table 3. AUXR Register
AUXR Register (SFR:8Eh)

AUXR	7	6	5	4	3	2	1	0
T89C51RD2 Reset value: xxxx xx00b	-	-	M0	-	XRS1	XRS0	EXTRAM	A0
AT89C51RD2/ED2 Reset value: 0x0x 000'HSB.XRAM'0b	DPU	-	M0	XRS2	XRS1	XRS0	EXTRAM	A0

AT89C51RD2/ED2 introduces several new bits, for internal XRAM sizing, stretch MOVX and disable weak pull-up (see AT89C51RD2/ED2 datasheet for details). The default configuration is compatible with T89C51RD2, therefore no special modification is needed.

Table 4. AUXR1 Register
AUXR1 Register (SFR:A2h)

AUXR1	7	6	5	4	3	2	1	0
T89C51RD2 Reset value: xxxx x0x0b	-	-	-	-	GF3	0	-	DPS
AT89C51RD2/ED2 Reset value: xxxx x0x0b	-	-	ENBOOT	-	GF3	0	-	DPS

AT89C51RD2/ED2 features the ENBOOT bit to map the ROM bootlloader area in the logical addressable space of the microcontroller. This special bit must be set before calling the common API entry point in the bootloader. Thus if the software application calls the API from the bootloader, the API call sequence must be modified (set ENBOOT before the “LJMP 0FFF0h” instruction).

Table 5. CKCON0 Register
CKCON0 Register (SFR:8Fh)

CKCON0	7	6	5	4	3	2	1	0
T89C51RD2 Reset value: x000 0000b	-	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2
AT89C51RD2/ED2 Reset value: 0000 0000b	SPIX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

The CKON register has been renamed to CKON0 register in AT89C51RD2/ED2. It introduces a new bit (SPIX2) to access the X2 mode of the SPI interface. If the application ignores this bit, no code modification is needed.

Table 6. EECON Register
EECON Register (SFR:D2h)

EECON	7	6	5	4	3	2	1	0

Table 6. EECON Register
EECON Register (SFR:D2h)

T89C51RD2 Reset value: 0000 xx00b	EEPL3	EEPL2	EEPL1	EEPL0	-	-	EEE	EEBUSY
AT89C51ED2 Reset value: xxxx xx00b	-	-	-	-	-	-	EEE	EEBUSY

The EECON register has been modified in AT89C51RD2/ED2. This implies code modification for write access to the on-chip EEPROM data of AT89C51ED2 device (see Figure 2 for typical write sequence).

The on-chip EEPROM data read access operation in AT89C51ED2 is the same as in T89C51RD2 (see Figure 3 for a typical read sequence).

Table 7. IEN0 Register
IEN0 Register (SFR:A8h)

IEN0	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
T89C51RD2 Reset value: 0000 0000b	EA	EC	ET2	ES	ET&	EX1	ET0	EXO
AT89C51RD2/ED2 Reset value: 0000 0000b	EA	EC	ET2	ES	ET&	EX1	ET0	EXO

The IE register has been renamed to IEN0 register in AT89C51RD2/ED2.

Table 8. IPL0Register
IPL0 Register (SFR:B8h)

IPL0	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
T89C51RD2 Reset value: 0000 0000b	-	PPCL	PT2L	PLS	PT1L	PX1L	PT0L	PX0L
AT89C51ED2 Reset value: 0000 0000b	-	PPCL	PT2L	PLS	PT1L	PX1L	PT0L	PX0L

The IPL register has been renamed to IPL0 register in AT89C51RD2/ED2.

Table 9. IPH0Register
IPH0 Register (SFR:B7h)

IPH0	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
T89C51RD2 Reset value: 0000 0000b	-	PPCH	PT2H	PHS	PT1H	PX1H	PT0H	PX0H
AT89C51RD2/ED2 Reset value: 0000 0000b	-	PPCH	PT2H	PHS	PT1H	PX1H	PT0H	PX0H

The IPH register has been renamed to IPH0 register in AT89C51RD2/ED2.

New Registers

In T89C51RD2, the memory locations of the new registers were previously unused. Thus migrating from T89C51RD2 to the new AT89C51RD2/ED2 does not require code modification for these SFR addresses.

Prescaler System

The prescaler interface uses the SFR: CKRL (SFR:97h)

Baud Rate Generator These registers are used for the Baud Rate Generator: BDRCON (SFR:9Bh), BRL (SFR:9Ah).

SPI Interface The SPI interface uses the registers: SPCON (SFR:C3h), SPSTR (SFR:C4h), SPDAT (SFR:C5h).

Keyboard Interface These registers control the keyboard interface: KBLS (SFR:9Ch), KBE (SFR:9Dh), KBF (SFR:9Eh).

New Interrupt Controller The IPL1 (SFR:B2h), IPH1 (SFR:B3h), IEN1 (SFR: B1h).

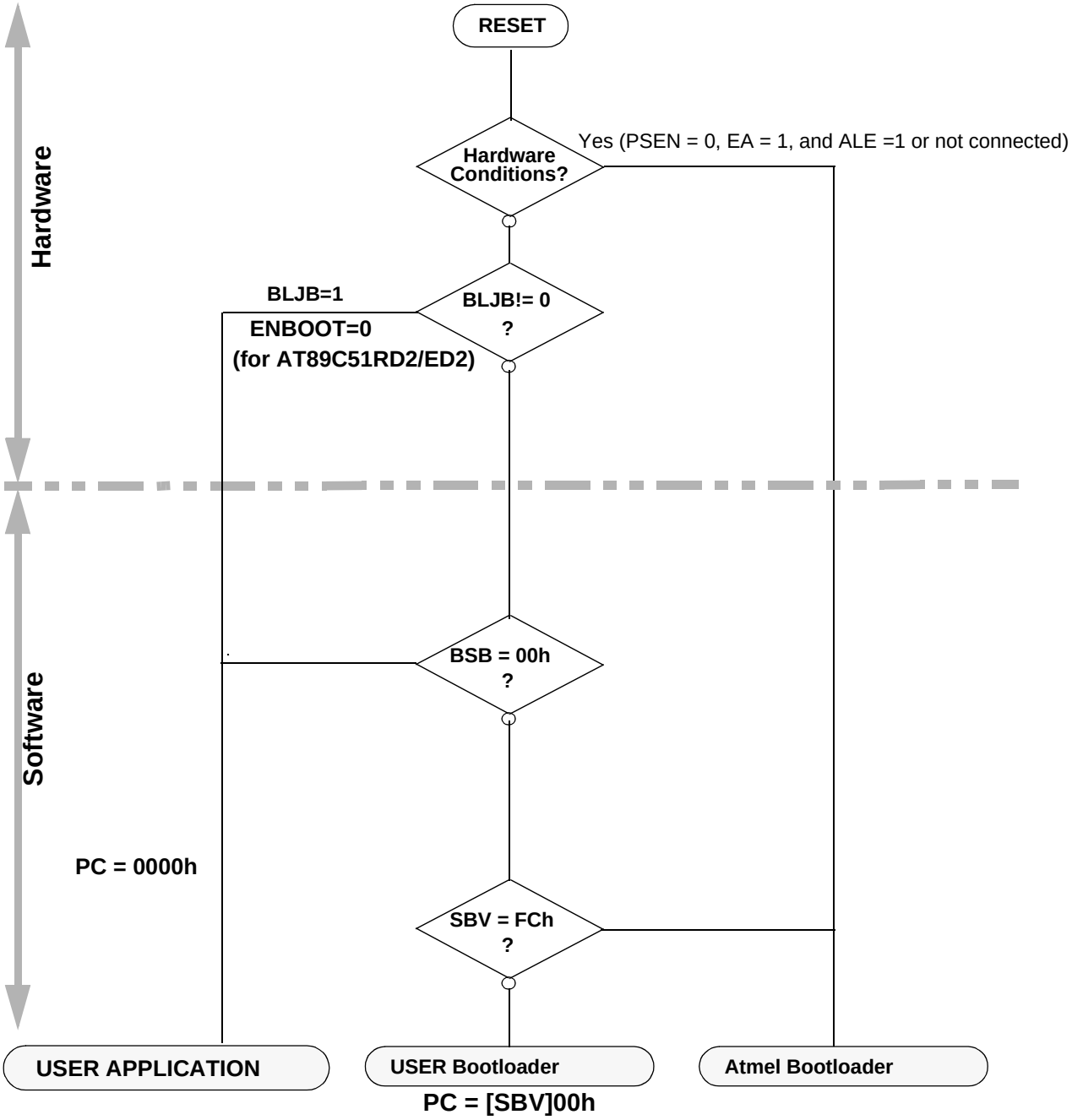
Bootloader Behavior

In-System Programming Features

Bootloader Activation

Both products have the same boot process (see Figure 4), Serial ISP can be activated in two ways: hardware or software conditions (according to BLJB, and BSB values).

Figure 4. Boot Process



ISP Commands

The serial ISP protocol for AT89C51RD2/ED2 is very similar to the T89C51RD2.

Table 10 summarizes the ISP commands for T89C51RD2 and AT89C51RD2/ED2, highlighted cells indicate the commands that differ between the two products.

Table 10. ISP Commands Comparison Table

Command	Command Name	Data[0]	Data[1]	Command Function	
				T89C51RD2	AT89C51RD2/ED2
00h	Program Data			Program Nb Data Byte. Bootloader will accept up to 16 (10h) data bytes. The data bytes should be 128 byte page Flash boundary.	Same as for T89C51RD2 except that the command allows up to 128 (80h) data bytes.
03h	Write Function	01h	00h	Not Implemented	Erase block0 (0000h-1FFFh)
			20h		Erase block1 (2000h-3FFFh)
			40h		Erase block2 (4000h-7FFFh)
			80h		Erase block3 (8000h- BFFFh)
			C0h		Erase block4 (C000h- FFFFh)
		03h	00h		Hardware Reset
			01h		Ljmp Address (data[2:3]= Address)
		04h	00h	Erase SBV & BSB	Same as T89C51RD2
		05h	00h	Program SSB level 1	
			01h	Program SSB level 2	
		06h	00h	Program BSB (value to write in data[2])	
			01h	Program SBV (value to write in data[2])	
		07h	-	Full Chip Erase	
		0Ah	04h	Not Implemented	Program BLJB fuse (value to write in data[2])
			08h		Program X2 fuse (value to write in data[2])
04h	Display Function	Data[0:1] = start address Data [2:3] = end address Data[4] = 00h -> Display data Data[4] = 01h -> Blank check		Display Data	Same as T89C51RD2
				Blank Check	

Table 10. ISP Commands Comparison Table (Continued)

Command	Command Name	Data[0]	Data[1]	Command Function	
				T89C51RD2	AT89C51RD2/ED2
05h	Read Function	00h	00h	Manufacturer Id	Same as T89C51RD2
			01h	Device Id #1	
			02h	Device Id #2	
			03h	Device Id #3	
		07h	00h	Read SSB	Same as T89C51RD2, but return value is different
			01h	Read BSB	Same as T89C51RD2
			02h	Read SBV	
			03h	Read Hardware Byte	Not Implemented
			06h	Not Implemented	Read Extra Byte
		08h	00h	Read Bootloader Version	Not Implemented
		0Bh	00h	Not Implemented	Read Hardware Byte
		0Eh	00h	Read Device Boot ID1	Same as T89C51RD2
			01h	Read Device Boot ID2	
		0Fh	00h	Not Implemented	Read Bootloader Version

The commands: “Read Hardware Byte” and “Read Bootloader Version” have a different transmission frame from T89C51RD2 to AT89C51RD2/ED2.

The ISP command “Read SSB” is the same, but the returned value is different. In fact the SSB byte has different coding value from T89C51RD2 to AT89C51RD2/ED2. Table 11 shows the coding values for SSB byte in both products.

Table 11. Cross Reference SSB Values

Software Security Level	SSB Value	
	T89C51RD2	AT89C51RD2/ED2
0	0xFF	0xFF
1	0x10	0xFE
2	0x00	0xFC

Note: FLIP is a PC software application running under Windows® 9X/2000/XP, Windows NT® and LINUX® that supports both products and makes the ISP protocol differences transparent for the end-user. This software is available from the Atmel web site.

In-Application Programming Capabilities (Self-Programming)

The AT89C51RD2/ED2 implements all API from the T89C51RD2 and a set of new functionalities.

The API entry point is similar in both products (“LCALL FFF0h”) in the bootloader. The major modification deals with the memory management. It is required to enable the ROM bootloader area before calling the common entry point (see Figure 5).

Figure 5. Recommended API Call Sequence

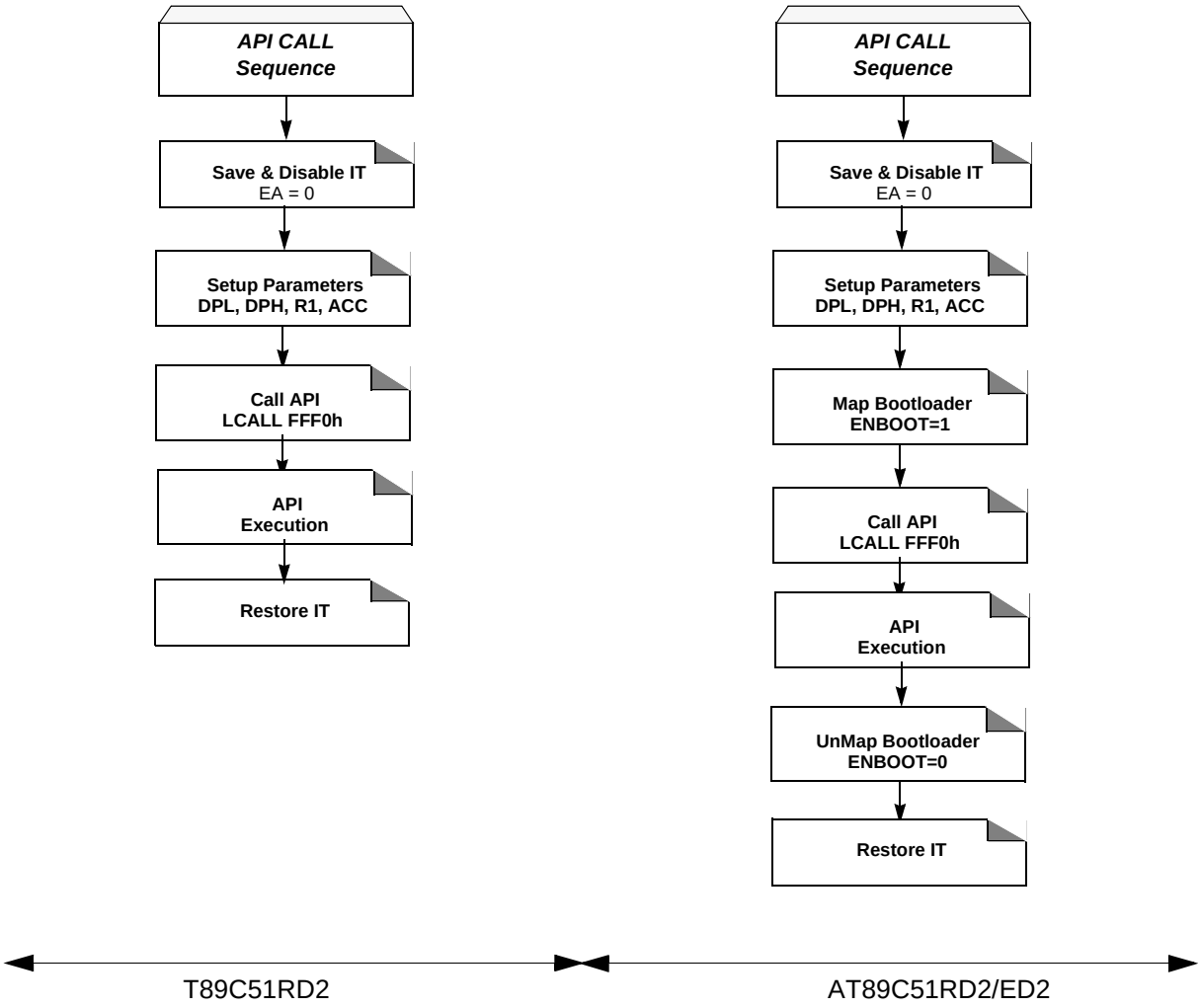


Table 12 summarizes the API calls for both products, greyed cells highlight API with different behavior from T89C51RD2 to AT89C51RD2/ED2.

Table 12. API Call Comparison Table

Command	R1	A	DPTR0	DPTR1	Returned Value	Command Effect	
						T89C51RD2	AT89C51RD2/ED2
READ MANUF ID	00h	XXh	0000h	XXh	ACC = Manufacturer ID	Read Manufacturer identifier	Same as T89C51RD2
READ DEVICE ID1	00h	XXh	0001h	XXh	ACC = Device ID1	Read Device identifier 1	
READ DEVICE ID2	00h	XXh	0002h	XXh	ACC = Device ID2	Read Device identifier 2	
READ DEVICE ID3	00h	XXh	0003h	XXh	ACC = Device ID3	Read Device identifier 3	
ERASE BLOCK	01h	XXh	DPH = 00h	00h	ACC = DPH	Not implemented	Erase block 0
			DPH = 20h				Erase block 1
			DPH = 40h				Erase block 2
			DPH = 80h				Erase block 3
			DPH = C0h				Erase block 4
PROGRAM DATA BYTE	02h	Byte value to program	Address of byte to program		ACC = 0: DONE	Program one Data Byte in user Flash	Same as T89C51RD2
ERASE BOOT VECTOR	04h	XXh	XXh	XXh	ACC = FCh	Erase Software boot vector and boot status byte. (SBV = FCh and BSB = FFh)	
PROGRAM SSB	05h	XXh	DPH = 00h DPL = 00h	00h	ACC = SSB value	Set SSB level 1	Same as T89C51RD2, but returned values are different See Table 11.
			DPH = 00h DPL = 01h			Set SSB level 2	
			DPH = 00h DPL = 10h			Set SSB level 0	
			DPH = 00h DPL = 11h			Set SSB level 1	
PROGRAM BSB	06h	New BSB value	0000h	XXh	none	Program boot status byte	Same as T89C51RD2
PROGRAM SBV	06h	New SBV value	0001h	XXh	none	Program software boot vector	
READ SSB	07h	XXh	0000h	XXh	ACC = SSB	Read Software Security Byte	Same as T89C51RD2, but returned values are different. See Table 11.
READ HSB	07h	XXh	0004h	XXh	ACC = HSB	Read Hardware Byte	Same as T89C51RD2
READ BSB	07h	XXh	0001h	XXh	ACC = BSB	Read Boot Status Byte	
READ SBV	07h	XXh	0002h	XXh	ACC = SBV	Read Software Boot Vector	

Table 12. API Call Comparison Table (Continued)

Command	R1	A	DPTR0	DPTR1	Returned Value	Command Effect	
						T89C51RD2	AT89C51RD2/ED2
READ BOOT VERSION	08h	XXXXh	XXh	XXh	ACC = Boot_Version	Read bootloader version	Not Implemented
PROGRAM DATA PAGE	09h	Number of byte to program	Address of the first byte to program in the Flash memory	Address in XRAM of the first data to program	ACC = 0: DONE	Program up to 128 bytes in user Flash. Remark: number of bytes to program is limited such as the Flash write remains in a single 128bytes page. Hence, when ACC is 128, valid values of DPL are 00h, or, 80h.	Same as T89C51RD2
PROGRAM X2 FUSE	0Ah	Fuse value 00h or 01h	0008h	XXh	none	Not implemented	Program X2 fuse bit with ACC
PROGRAM BLJB FUSE	0Ah	Fuse value 00h or 01h	0004h	XXh	none		Program BLJB fuse bit with ACC
READ BOOT ID1	0Eh	XXh	DPL=00h	XXh	ACC = ID1	Read boot ID1	Same as T89C51RD2
READ BOOT ID2	0Eh	XXh	DPL=01h	XXh	ACC = ID2	Read boot ID2	
READ BOOT VERSION	0Fh	XXh	XXXXh	XXh	ACC = Boot_Version	Not implemented	Read bootloader version

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